



MAIL DATE CANCELLED



EXPRESS MAIL NO. EL872037792US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Patent Application:

Applicant : Leland R. Nevill
Assignee : Micron Technology, Inc.
Filed : November 16, 2001
For : METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED CIRCUITS
Docket No. : 500060.02

Corresponding Issued U.S. Patent:

Patent No. : 5,984,190
Issued: : November 16, 1999
Application No. : 08/857,100
Filing Date : May 15, 1997
Examiner : Daniel St. Cyr
Art Unit : 2876

BOX REISSUE PATENT APPLICATION
Commissioner of Patents
Washington, DC 20231

PRELIMINARY AMENDMENT

Sir:

Please accept the request for a reissue of U.S. Patent No. 5,984,190, filed herewith. Prior to conducting the examination of the reissue claims, please amend the reissue application as follows:

Please add the following new claims 23-34:

- - 23. A method of identifying an integrated circuit, comprising:
programming the integrated circuit with an electronic identification information;
and
marking the integrated circuit with an optical identification code that corresponds
with the electronic identification information;
reading the electronic identification information; and
cross-referencing the optical identification code with the read electronic
identification information to associate the optical identification code with the corresponding
electronic identification information.

24. The method of claim 23 wherein the act of cross-referencing the optical
identification code with the read electronic identification information comprises:
reading the optical identification code; and
cross-referencing the read optical identification code with the read electronic
identification information.

25. The method of claim 23 wherein the act of cross-referencing the optical
identification code with the read electronic identification information comprises accessing a
lookup table containing the optical identification code and the read electronic identification
information.

26. The method of claim 23 wherein the act of programming the integrated
circuit with electronic identification information comprises programming at least one of a
plurality of programmable links.

27. The method of claim 23 wherein the act of marking the integrated circuit
with an optical identification code includes the step of placing an adhesive label on the integrated
circuit.

28. In an integrated circuit which includes a programmable circuit for storing an electronically readable identification code which identifies the integrated circuit, a method of identifying the integrated circuit, comprising the steps of:

marking the integrated circuit with an optical identification code;

reading the electronically readable identification code; and

comparing the optical identification code with the read electronically readable identification code to associate the optical identification code with the electronically readable identification code.

29. The method of claim 28 wherein the act of comparing the read electronically readable identification code with the optical identification code comprises:

creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an optical identification code; and

accessing the look-up table.

30. The method of claim 29 wherein the act of creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an optical identification code comprises creating a look-up table that uniquely associates the optical identification code for each of a plurality of integrated circuits with an optical identification code.

31. The method of claim 29 wherein the act of creating a look-up table that associates the optical identification code for each of a plurality of integrated circuits with an optical identification code comprises creating a look-up table that uniquely associates the optical identification code for each of a plurality of integrated circuits with an optical identification code.

32. An integrated circuit comprising an integrated circuit chip mounted within a package, the integrated circuit comprising:

an identification circuit fabricated on the integrated circuit chip, the identification circuit being operable to store identification data; and

an optical identification mark on the package of the integrated circuit, the optical identification mark encoding information corresponding to the identification data.

33. The integrated circuit of claim 32 wherein the programmable identification circuit includes a plurality of programmable links.

34. The integrated circuit of claim 33 wherein the optical identification mark encodes information identical to the identification data. - -

REMARKS

Consideration of this reissue application in view of the above amendments and following remarks is respectfully requested. Applicant is requesting reissue on the basis that the '190 patent is, through error without any deceptive intention, deemed wholly or partially inoperative by reason of the patentee claiming less than he had a right to claim in the '190 patent. For example, claim 1 of the '190 patent is limited to using a lookup table to associate the optical identification code with the corresponding electronic identification information, but applicant has a right to claim that other means may be used to associate the optical identification code with the corresponding electronic identification information. The assignee offers to surrender the '190 patent once the Examiner has indicated the allowability of all claims associated with this reissue application. The assignee is requesting a reissue of the '190 patent for the invention as disclosed in the '190 patent and claimed in issued claims 1-22 and new claims 23-34.

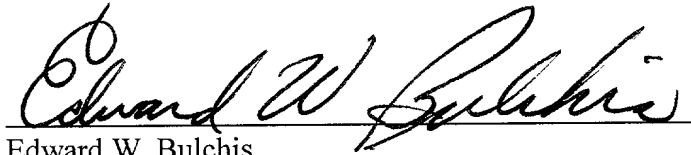
No new matter has been introduced into this application for reissue.

Applicant believes claims 1-34 are in condition for allowance and respectfully requests such action.

If there are any matters that can be handled in a telephone conversation, the Examiner is encouraged to contact Mr. Bulchis at (206) 903-8785.

Respectfully submitted,

DORSEY & WHITNEY LLP

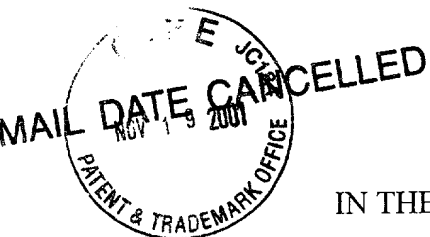
A handwritten signature in black ink, reading "Edward W. Bulchis". The signature is written in a cursive style with a large, stylized "E" at the beginning.

Edward W. Bulchis
Registration No. 26,847

EWB:mp

1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101-4010
(206) 903-8800
Fax: (206) 903-8820

H:\IP\Documents\Clients\Micron Technology\00\500060.02\500060.02 reissue pam.doc



EXPRESS MAIL NO. EL872037792US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reissue Patent Application:

Applicant : Leland R. Nevill
Assignee: : Micron Technology, Inc.
Filed : November 16, 2001
For : METHOD AND APPARATUS FOR IDENTIFYING INTEGRATED
CIRCUITS
Docket No. : 500060.02

Corresponding Issued U.S. Patent:

Patent No. : 5,984,190
Issued : November 16, 1999
Application No. : 08/857,100
Filing Date : May 15, 1997
Examiner : Daniel St. Cyr
Art Unit : 2876
Date : November 9, 2001

BOX REISSUE

Commissioner of Patents and Trademarks
Washington, DC 20231

FILING FORMAL DRAWINGS IN REISSUE APPLICATION

Sir:

Enclosed are the drawings from the original file of U.S. Patent No. 5,984,190 to be used for the reissue application of U.S. Patent No. 5,984,190. There are no changes in the drawings for the reissue application.

Respectfully submitted,

Dorsey & Whitney LLP

Edward W. Bulchis
Registration No. 26,847

Enclosures:

1 Sheet of Drawings, Figures 1-3

1420 Fifth Avenue, Suite 3400
Seattle, Washington 98101
(206) 903-8800 Fax: (206) 903-8820